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06EC45

Fourth Semester B.E. Degree Examination, January 2013
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain how data types are classified in HDL. Mention the advantages of VHDL data types over verilog. **(06 Marks)**

b. Explain composite and access data types with an example for each. **(08 Marks)**

c. Discuss the logical operators in VHDL. **(06 Marks)**

2 a. Explain signal declaration and signal assignment statements with relavant examples. **(06 Marks)**

b. Write a dataflow description (in both VHDL and verilog) for a full-adder with active high enable. **(08 Marks)**

c. Write HDL codes for 2 × 2 bit combinational array multiplier. **(06 Marks)**

3 a. Write behavioral description of a half-adder in VHDL and verilog with propagation delay of 5 nsec. Discuss the important features of their description in VHDL and verilog. **(08 Marks)**

b. Explain the execution of process statement. **(02 Marks)**

c. Write VHDL code for a D latch using variable assignment statement and signal assignment statements. With simulation waveforms clearly distinguish between the two statements. **(10 Marks)**

4 a. What is binding? Discuss the binding between library and components. **(08 Marks)**

b. Write the HDL description of 2:1 mutliplexer with active low enable in VHDL/verilog using structural style. **(12 Marks)**

PART – B

5 a. Explain the following syntax with examples:
i) Procedure
ii) Task
iii) Function. **(06 Marks)**

b. Write VHDL/verilog code to convert a fractional binary to real number using procedures/tasks. **(08 Marks)**

c. Describe all file processing tasks in verilog. **(06 Marks)**

6 a. What is the necessity of mixed type description? **(04 Marks)**

b. Describe the development of HDL code for an ALU and write VHDL/verilog code for an ALU shown below.

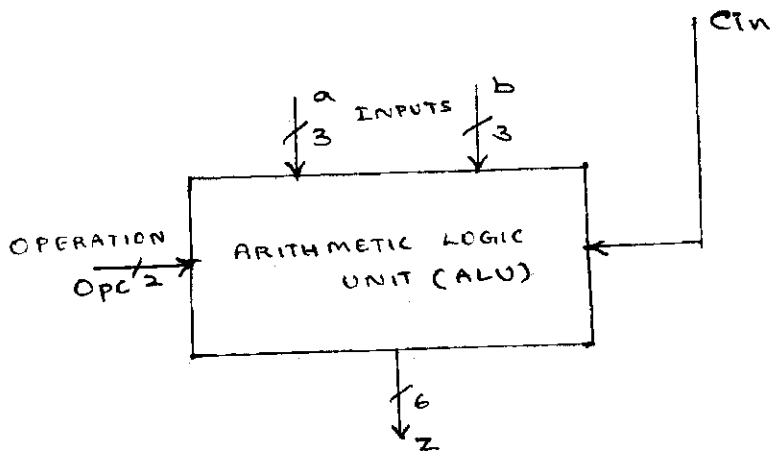

Fig.Q.6(b)

Assume the following operations: Addition, multiplication, division, no operation. **(16 Marks)**

7 a. How to invoke a verilog module from VHDL module? Explain with an example of a mixed language description for a full adder using two half adders. **(10 Marks)**

b. Write a mixed language description of a 4-bit adder with zero flag. **(10 Marks)**

8 a. What is synthesis? List the general steps involved in synthesis. **(08 Marks)**

b. Give synthesis information extracted, when the input and output are defined as:
i) bit; ii) std-logic-vector. **(04 Marks)**

c. Write a behavirourl code in VHDL and verilog for the signal assignment statement B = A. Explain the mapping to gate level logic diagram. **(08 Marks)**

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